I. Amendments to the Claims

1. (Previously Presented) An integrated circuit arrangement, comprising:

an electrically insulating insulating region, and

at least one sequence of regions which forms a capacitor and which contains, in the order specified:

an electrode region near the insulating region,

a dielectric region, and

an electrode region remote from the insulating region,

the insulating region being part of an insulating layer arranged in a plane,

the capacitor and at least one active component of the integrated circuit arrangement being arranged on the same side of the insulating layer,

the electrode region near the insulating region and an active region of the component being arranged in a plane which lies parallel to the plane in which the insulating layer is arranged, and

the capacitor and the active component forming a memory cell,

wherein at least one processor is contained in the integrated circuit arrangement.

2. (Currently Amended) The circuit arrangement as claimed in claim 1, further comprising at least one field-effect transistor, wherein at least one of:

a channel region of the transistor is the active region,

a control electrode of the transistor at least one of contains the same material or material of the same dopant concentration as the electrode region remote from the insulating region,

~~a control electrode insulating region at least one of contains the same material or a material having the same thickness as the dielectric region, or~~

~~the~~ a control electrode insulation region ~~at least one of~~ contains containing a different material ~~or a material having a different thickness~~ than the dielectric region.

3. (Previously Presented) The circuit arrangement as claimed in claim 2, wherein at least one of:

the field-effect transistor is a planar field-effect transistor,

the transistor contains auxiliary terminal regions, which have a doping with the same conduction type as terminal regions of the transistor but with a dopant concentration that is smaller by at least one order of magnitude,

the transistor contains auxiliary doping regions, which are arranged at least one of near the terminal regions or near the auxiliary terminal regions and which have a doping with a different conduction type at least one of than the terminal regions or than the auxiliary terminal regions, or

the control electrode adjoins a region containing a metal-semiconductor compound.

4. (Previously Presented) The circuit arrangement as claimed in claim 3, wherein at least one of:

one terminal region of the transistor or both terminal regions of the transistor adjoin the insulating layer,

at least one terminal region adjoins a region containing a metal-semiconductor compound,

a boundary area of at least one terminal region which is remote from the insulating region is further away from the insulating layer than the active region, or

a boundary area of at least one terminal region which is remote from the insulating region is arranged nearer to the insulating layer than a boundary area of the active region which is remote from the insulating region.

5. (Previously Presented) The circuit arrangement as claimed in claim 2, wherein at least one of:

spacers are arranged on both sides of the control electrode, and the spacers comprise a different material than the control electrode,

a spacer is arranged at at least one side of the electrode region remote from the insulating region, and the spacer comprises a different material than the electrode region remote from the insulating region or

a spacer arranged at the control electrode and a spacer arranged at the electrode region remote from the insulating region touch one another.

6. (Previously Presented) The circuit arrangement as claimed in claim 2, wherein at least one of:

a terminal region of the field-effect transistor and the electrode region of the capacitor which is near the insulating region adjoin one another and have an electrically conductive connection at the boundary,

the terminal region of the transistor which adjoins the electrode region near the insulating region does not adjoin a region containing a metal-semiconductor compound, or

wherein another terminal region of the transistor adjoins a region containing a metal-semiconductor compound.

7. (Previously Presented) The circuit arrangement as claimed in claim 6, wherein:

a side of the electrode region near the insulating region which adjoins the terminal region is longer than a side of the electrode region near the insulating region which lies transversely with respect to said side near the insulating region, or

wherein the side of the electrode region near the insulating region which lies transversely with respect to the side of the electrode region near the

insulating region which adjoins the terminal region is longer than the side adjoining the terminal region.

8. (Currently Amended) The circuit arrangement as claimed in claim 1, wherein at least one of:

the electrode region near the insulating region is a monocrystalline region,

at least one of the electrode region near the insulating region or the active region has a thickness of less than 100 nanometers,

the active region is a monocrystalline region,

the insulating layer adjoins, at one side, a carrier substrate,

the insulating layer adjoins the electrode region near the insulating region at a side other than the side at which the insulating layer adjoins the carrier substrate,

the boundary areas lie completely in two mutually parallel planes,

the insulating layer comprises an electrically insulating material, or

the active component is a transistor.

9. (Previously Presented) The circuit arrangement as claimed in claim 1, wherein at least one of:

the dielectric region comprises silicon dioxide,

the dielectric region comprises a material having a dielectric constant of greater than 4,

the electrode region remote from the insulating region comprises silicon,

the electrode region remote from the insulating region comprises a metal,

the electrode region remote from the insulating region contains a low-impedance material, or

the electrode region remote from the insulating region adjoins a region containing metal-semiconductor compounds.

10. (Previously Presented) The circuit arrangement as claimed in claim 1, wherein at least one of:

the processor,is a microprocessor,

the capacitor and the active component form a memory cell, or

a memory cell contains either a capacitor and only one transistor or a capacitor and more than one transistor.

11. (Currently Amended) A method for fabricating an integrated circuit arrangement with a capacitor, a transistor, and a processor, in which the following method steps are performed without any restriction by the order specified:

providing a substrate containing an insulating layer made of electrically insulating material and a semiconductor layer, the insulating layer being planar and having an electrically insulating insulating region,

patterning the semiconductor layer in order to form at least one electrode region near the insulating region for the capacitor and in order to form at least one active region for the transistor,

after the patterning of the semiconductor layer, producing at least one dielectric layer,

after the production of the dielectric layer, producing an electrode layer), and

forming an electrode of the capacitor which is remote from the insulating region in the electrode layer,

wherein the capacitor and the transistor are arranged on the same side of the insulating layer,

the electrode region near the insulating region and the active region of the transistor are arranged in a plane which lies parallel to the plane in which the insulating layer is arranged, and

the capacitor and the transistor form a memory cell in conjunction with a processor.

12. (Previously Presented) The method as claimed in claim 11, further comprising at least one of the following steps:

applying at least one auxiliary layer to the semiconductor layer prior to patterning,

doping a channel region of the transistor,

carrying out of a thermal oxidation in order to form a rounding oxide,

doping the electrode near the insulating region,

producing the dielectric layer at the same time as a dielectric layer at the active region of the transistor, or

forming a control electrode of the transistor at the same time as the formation of the electrode region remote from the insulating region.

13. (Previously Presented) The method as claimed in claim 11, further comprising at least one of the following steps:

forming auxiliary terminal regions with a lower dopant concentration than terminal regions of the transistor,

forming auxiliary doping regions,

applying a further auxiliary layer after the patterning of a control electrode of the transistor, or

anisotropically etching the further auxiliary layer.

14. (Previously Presented) The method as claimed in claim 11, further comprising at least one of the following steps:

carrying out of a selective epitaxy on uncovered regions made of semiconductor material at least one of after the formation of the electrode region remote from the insulating region or after the patterning of a control electrode of the transistor, or

doping terminal regions of the transistor at least one of after the formation of the electrode region remote from the insulating region or after the patterning of the control electrode.

15. (Previously Presented) The method as claimed in claim 11, further comprising the following step: selectively forming a metal-semiconductor compound at least one of on the electrode layer or on uncovered semiconductor regions.